CLAIMS

1. A phase lock loop comprising:

a detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal;

a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector; and

wherein the timing reference signal generator is operatively configured to produce an output signal at a characteristic frequency an integral multiple of a desired output clock frequency.

2. The phase lock loop according to claim 1, further comprising a frequency divider circuit coupled to receive the output signal and reduce its characteristic frequency to a desired output clock frequency.

3. The phase lock loop according to claim 2, further comprising a loop filter coupled between the phase/frequency detector and the timing reference generator, the loop filter developing a control voltage for the timing reference generator.

4. The phase lock loop according to claim 2, wherein the timing reference generator is constructed to output multi-phase signals, each phase signal oscillating at the characteristic frequency.

5. The phase lock loop according to claim 4, further comprising a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal.

6. The phase lock loop according to claim 5, wherein the timing reference signal generator is operatively configured to produce an output signal at a characteristic frequency M times the frequency of a desired output clock frequency.

7. The phase lock loop according to claim 6, wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

8. The phase lock loop according to claim 7, wherein the phase select MUX is a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence.

9. The phase lock loop according to claim 8, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

10. The phase lock loop according to claim 9, wherein the frequency divider circuit is constructed of current mode logic components.

11. The phase lock loop according to claim 9, wherein the phase control MUX is constructed of current mode logic components.

12. A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a frequency characteristic of an input signal to a frequency characteristic

of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator responsive, in feedback fashion, to said control signals asserted by the comparison circuit; and

wherein the timing reference signal generator is configured to develop an output signal at a frequency M times the frequency of a desired output clock signal.

13. The timing circuit according to claim 12, wherein the desired output clock signal has a frequency characteristic N times the frequency characteristic of the input signal.

14. The timing circuit according to claim 13, further comprising:

first frequency divider circuitry disposed between the timing reference signal generator and the comparison circuit; and

second frequency divider circuitry disposed between the timing reference signal generator and an output, wherein the first and second frequency divider circuitry having different frequency division characteristics.

15. The timing circuit according to claim 14, the first frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor (NxM) to develop said frequency characteristic provided to said comparison circuit.

16. The timing circuit according to claim 15, the second frequency divider circuitry dividing the output signal of the

timing reference signal generator by a scale factor M to develop said desired output clock signal.

17. The timing circuit according to claim 16, wherein the timing reference signal generator is implemented as a VCO, the VCO constructed as a sequential delay stage.

18. The timing circuit according to claim 17, the VCO developing multi-phase output signals, each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage.

19. The timing circuit according to claim 18, wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

20. The timing circuit according to claim 18, further comprising a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal.

21. The timing circuit according to claim 20, wherein the phase select MUX is a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence.

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22. The timing circuit according to claim 21, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

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